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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/515,158	02/29/2000	John M. Quernemoen	RA-5247	1831

7590 06/21/2002

Charles A Johnson
UNISYS Corporation
M S 4773
P O Box 64942
St Paul, MN 55164-0942

EXAMINER
DODDS, HAROLD E

ART UNIT	PAPER NUMBER
2177	

DATE MAILED: 06/21/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/515,158	Applicant(s) QUERNEMOEN ET AL.
	Examiner Harold E. Dodds, Jr.	Art Unit 2177

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☒ Claim(s) *2 and 4-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 February 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. The attempt to incorporate subject matter into this application by reference to "Co-Pending Applications" is improper because the U.S. Patent Application Numbers and filing dates have not been supplied.

Correction is required.

Claim Objections

2. Claim 4 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 2. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Correction is required.

3. The referencing clauses in the claims are not in accordance with 37 CFR 1.75(c), which requires that a claim may refer back to and further limit another claim. Claims 4-15 are objected to because of the following informalities: Claim 4 states "...a method as recited in claim 4...".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over DeLuca et al. (U.S. Patent No. 5,848,270), Litzenberger (U.S. Patent No. 5,870,460), and Shannon et al. (U.S. Patent No. 6,088,678).

6. DeLuca rendered obvious independent claim 1 by the following:

"...providing one or more percent...utilization limits..." at col. 12, lines 6-10.

"...hardware..." at col. 5, lines 30-33.

"...while remaining within the percent...utilization limits..." at col. 12, lines 6-10.

"...hardware..." at col. 5, lines 30-33.

"...hardware..." at col. 5, lines 30-33.

DeLuca does not teach the use of throughput workload requirements and calculating the required resources.

7. However, Litzenberger teaches the use of throughput workload requirements as follows:

"...obtaining throughput...requirements..." at col. 2, lines 4-8.

"...workload..." at col. 3, lines 27-29.

"...needed to satisfy the...requirements..." at col. 2, lines 4-8.

"...workload..." at col. 3, lines 27-29.

It would have been obvious to one ordinarily skilled in the art at the time of the invention to use throughput workload requirements in order to determine how much work the computer hardware would be required to perform to justify hardware upgrades.

Litzenberger does not teach calculating the required resources.

8. However, Shannon teaches the use of calculating the required resources as follows:

"...calculating the...resources..." at col. 1, lines 66-67 and col. 2, lines 1-6.

It would have been obvious to one ordinarily skilled in the art at the time of the invention to calculate the hardware resources required for a system in order to estimate the cost of hardware upgrades.

9. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeLuca, Litzenberger, and Shannon as applied to claim 1 above, and further in view of Kayahara (U.S. Patent No. 6,405,206). Claim 4 has been assumed to be dependent on claim 1 for this office action.

As per claims 2 and 4, the "...to the percent...utilization limits...," is taught by DeLuca at col. 12, lines 6-10,

the "...hardware...," is taught by DeLuca at col. 5, lines 30-33,

the "...recalculating the required...resources...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6,

the "...hardware...," is taught by DeLuca at col. 5, lines 30-33,

the "...in order to remain within said percent...utilization limits...," is taught by DeLuca at col. 12, lines 6-10,

the "...hardware...," is taught by DeLuca at col. 5, lines 30-33,

the "...the required...resources...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6,

the "...hardware...," is taught by DeLuca at col. 5, lines 30-33,

but the "...accepting user entered changes ...,"

and the "...outputting...to the human user in a format to advise the human user...," are

not taught by either DeLuca, Litzenberger, or Shannon.

However, Kayahara teaches the use of user input and the outputting of data in

formats as follows:

"...An information search processing device in accordance with the invention comprises memory means that stores multiple types of searching strategies that show ways of information searching, user input controlling means that accepts a searching request of a user, reads out the multiple types of searching strategies from said memory means, and displays them on a display means to enable the user to select an arbitrary searching strategy among the multiple types of searching strategies, and searching means that performs information searching with respect to the searching request which was input by the user in accordance with the searching strategy which is selected by the user..." at col. 3, lines 25-37.

"...Therefore, it is an object of the invention to dramatically decrease the burden of the searching operation which is performed by the user, make information searching possible by a searching method which the user desires, and make it possible to output a search result by categorizing and coordinating into a format the user desires..." at col. 1, lines 59-64.

It would have been obvious to one ordinarily skilled in the art at the time of the invention to allow user input and to output the results of the calculations in a defined format in order to provide the user with the capability of changing the previously defined data and to provide the user feedback in a meaningful format.

10. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over DeLuca, Litzenberger, and Shannon as applied to claim 1 above, and further in view of Oulid-Aissa et al. (U.S. Patent No. 5,835,757).

As per claim 3, the "...obtaining...requirements...," is taught by Shannon at col. 1, lines 13-18,

the "...and calculating the...resources ...," is taught by Shannon at col 1, lines 66-67 and col. 2, lines 1-6,

the "...hardware...," is taught by DeLuca at col. 5, lines 30-33,

the "...while remaining within the percent...utilization limits...," is taught by DeLuca at col. 12, lines 6-10,

the "...hardware...," is taught by DeLuca at col. 5, lines 30-33,

but the "...database requirements..."

and the "...needed to satisfy the database requirements...," are not taught by either DeLuca, Litzenberger, or Shannon.

However, Oulid-Aissa teaches the use of database requirements as follows:

"...New database requirements impacting data structures, contents, or access techniques may then be added without impact to the applications..." at col. 5, lines 52-54.

It would have been obvious to one ordinarily skilled in the art at the time of the invention to use database requirements when defining a computer system in order to provide a means of storing data used by the application programs.

11. Claims 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeLuca, Litzenberger, Shannon, and Kayahara as applied to claim 4 above, and further in view of Kulkarni et al. (U.S. Patent No. 6,138,016).

As per claim 5, the "...throughput...requirement...,"is taught by Litzenberger at col. 2, lines 4-8,

the "...workload...," is taught by Litzenberger at col. 3, lines 27-29,

but the "...includes a transactions per second requirement...," is not taught by either DeLuca, Litzenberger, Shannon, or Kayahara.

However, Kulkarni teaches the use of the transactions per second requirement as follows:

"...To overcome the requirement of localizing the HLR in a single expensive machine, with a very high rate of messages per second and data base transactions per second, and according to this invention, the HLR function is distributed across multiple processors..." at col. 1, lines 58-62.

It would have been obvious to one ordinarily skilled in the art at the time of the invention to use the measure transactions per second for workload throughput in order to use a widely used measure and gain acceptance for this method of sizing computer hardware requirements.

12. As per claim 6, the "...calculating and recalculating steps include calculating the...resources needed...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6,

the "...hardware...," is taught by DeLuca at col. 5, lines 30-33,

and the "...as a function of the transactions per second...," is taught by Kulkarni at col. 1, lines 58-62.

13. As per claim 7, the "...hardware...," is taught by DeLuca at col. 5, lines 30-33,

the "...resource...," is taught by Litzenberger at col. 2, lines 14-18,

the "...requirements...," is taught by Litzenbergrer at col. 2, lines 4-8,

and the "...include a number of processors...," is taught by Kulkarni at col. 2, lines 13-29.

14. As per claim 8, the "...calculating and recalculating steps include calculating...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6, the "...said number of processors...," is taught by Kulkarni at col. 2, lines 13-29, and the "...as a function of the transactions per second...," is taught by Kulkarni at col. 1, lines 58-62.

15. As per claim 9, the "...percent...utilization limits include percent...utilization...," is taught by DeLuca at col. 12, lines 6-10, the "...hardware...," is taught by DeLuca at col. 5, lines 30-33, the "...processor...," is taught by Kulkarni at col. 2, lines 13-29, the "...and said accepting step includes accepting changes...," is taught by Kayahara at col. 3, lines 25-37, the "...to said...utilization...," is taught by DeLuca at col. 12, lines 6-10, the "...processor...," is taught by Kulkarni at col. 2, lines 13-29, the "...and said calculation and recalculation steps includes calculating...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6, the "...said hardware...,"is taught by Deluca at col. 5, lines 30-33, the "...requirements...," are taught by Litzenberger at col. 2, lines 4-8, the "...within said...utilization limits...," is taught by DeLuca at col. 12, lines 6-10, the "...processor...," is taught by Kulkarni at col. 2, lines 13-29, the "...and include changing said number of processors required...," is taught by Kulkarni at col. 2, lines 13-29,

the "...when necessary to remain within said...utilization limits...," is taught by DeLuca at col. 12, lines 6-10,

and the "...processor...," is taught by Kulkarni at col. 2, lines 13-29.

16. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeLuca, Litzenberger, Shannon, Kayahara, and Kulkarni as applied to claim 9 above, and further in view of Itoh et al. (U.S. Patent No. 5,802,308) and Obhan (U.S. Patent No. 6,275,695).

As per claim 10, the "...processor...," is taught by Kulkarni at col. 2, lines 13-29,

the "...utilization limits...," is taught by DeLuca at col. 12, lines 6-10,

the "...and said calculating and recalculating steps include calculating...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6,

the "...said number of processors needed...," is taught by Kulkarni at col. 2, lines 13-29,

the "...of said processors...," is taught by Kulkarni at col. 2, lines 13-29,

but the "...include upper utilization limits...,"

the "...to prevent over utilizing said processors...,"

the "...keeping below said upper limit..,"

and the "...to prevent over utilization...," are not taught by either DeLuca, Litzenberger, Shannon, Kayahara, or Kulkarni.

However, Itoh teaches the use of upper utilization limits and being under the upper limits as follows:

"...The upper and lower limit values are respectively designated as X1 and X2 for the utilization of the central control unit, Y1 and Y2 for the utilization of the shared resources, and Z1 and Z2 for the response processing time..." at col. 4, lines 59-63.

"...The effect of the control has now begun to show, and at time t4, the load or utilization drops below the upper limit but still above the lower limit, so that the level 3 is maintained..." at 6, lines 41-44.

It would have been obvious to one ordinarily skilled in the art at the time of the invention to set upper utilization limits on a processor and to operate below those limits in order to avoid overload of the system, and possibly have system failure.

Itoh does not teach the over utilization of processors.

However, Obhan teaches the over utilization of system resources as follows:

"...Each time the BTS resource reaches a BTS watermark a signal is sent to the SYM server 324 to apprise the SYM server 324 of such under or over utilization..." at col. 10, lines 54-57.

It would have been obvious to one ordinarily skilled in the art at the time of the invention to avoid overload of the system in order to prevent this cause of system failure.

17. As per claim 11, the "...processor...," is taught by Kulkarni at col. 2, lines 13-29,

the "...utilization limits...," is taught by DeLuca at col. 12, lines 6-10,

the "...include lower utilization limits...," is taught by Itoh at col. 4, lines 59-63,

the "...to prevent under utilizing...," is taught by Obhan at col. 10, lines 54-57,

and the "...said processors...," is taught by Kulkarni at col. 2, lines 13-29.

18. As per claim 12, the "...calculating and recalculating steps include calculating...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6,

the "...said number of processors needed...," is taught by Kulkarni at col. 2, lines 13-29,

the "...keeping above said lower limit...," is taught by Itoh at col. 6, lines 41-44,

the "...to prevent under utilization...," is taught by Obhan at col. 10, lines 54-57,

and the "...of said processors...," is taught by Kulkarni at col. 2, lines 13-29.

19. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeLuca, Litzenberger, Shannon, Kayahara, Kulkarni, Itoh, and Obhan as applied to claim 9 above, and further in view of Fletcher et al. (U.S. Patent No. 6,108,782).

As per claim 13, the "...percent...utilization limits include percent...utilization...," is taught by DeLuca at col. 12, lines 6-10,

the "...hardware...," is taught by DeLuca at col. 5, lines 30-33,

the "...and said calculating and recalculating steps include calculating...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6,

the "...said hardware...," is taught by DeLuca at col. 5, lines 30-33,

the "...requirements...," is taught by Litzenberger at col. 2, lines 4-8,

the "...utilization limits...," is taught by DeLuca at col. 12, lines 6-10,

the "...required when necessary to remain within...utilization limits...," is taught by DeLuca at col. 12, lines 6-10,

but the "...network interface card...,"

the "...within said network interface card...,"

the "...and include changing said number of network interface cards...,"

and the "...said network interface card...," are not taught by either DeLuca, Litzenberger, Shannon, Kayahara, Kulkarni, Itoh, or Obhan.

However, Fletcher teaches the use of network interface cards as follows:

"...According to the present invention, collectors and agents may be designed to operate effectively with a number of different network interface cards (NICs) and NOS architectures and a number of different management applications..." at col. 15, lines 61-64.

It would have been obvious to one ordinarily skilled in the art at the time of the invention to use network interface cards in order to communicate between processors in the system.

20. As per claim 14, the "...network interface card...," is taught by Fletcher at col. 15, lines 61-64,

the "...utilization limits...," is taught by DeLuca at col. 12, lines 6-10,

the "...include lower utilization limits...," is taught by Itoh at col. 4, lines 59-63,

the "...to prevent under utilizing...," is taught by Obhan at col. 10, lines 54-57,

the "...said network interface cards...," is taught by Fletcher at col. 15, lines 61-64,

the "...and said calculating and recalculating steps include calculating...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6,

"...said number of network interface cards...," is taught by Fletcher at col. 15, lines 61-64,

the "...needed keeping above said lower limit...," is taught by Itoh at col. 6, lines 41-44,

the "...to prevent under utilization...," is taught by Obhan at col. 10, lines 54-57,

"...of said network interface cards....," is taught by Fletcher at col. 15, lines 61-64.

21. As per claim 15, the "...network interface card...," is taught by Fletcher at col. 15, lines 61-64,

the "...utilization limits...," is taught by DeLuca at col. 12, lines 6-10,

the "...include upper utilization limits...," is taught by Itoh at col. 4, lines 59-63,

the "...to prevent over utilizing...," is taught by Obhan at col. 10, lines 54-57,

the "...said network interface cards...," is taught by Fletcher at col. 15, lines 61-64,

the "...and said calculating and recalculating steps include calculating...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6,

the "...said number of network interface cards needed...," is taught by Fletcher at col. 15, lines 61-64,

the "...keeping below said upper limit...," is taught by Itoh at col. 6, lines 41-44,

the "...to prevent over utilization...," is taught by Obhan at col. 10, lines 54-57,

and the "...of said network interface cards...," is taught by Fletcher at col. 15, lines 61-64.

22. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coss et al. (U.S. Patent No. 5,538,423), DeLuca, Shannon, Litzenberger, and Kulkarni.

23. Coss rendered obvious independent claim 16 by the following:

"...establishing default values..." at col. 19, lines 54-57.

"...for hardware..." at col. 19, lines 40-41.

"...initializing said hardware..." at col. 19, lines 40-41.

"...to said default values..." at col. 19, lines 54-57.

"...hardware..." at col. 19, lines 40-41.

"...hardware..." at col. 19, lines 40-41.

Cross does not teach the use of utilization limits, the obtaining requirements from users, the use of workloads, the calculating of requirements, and the use of functions.

24. However, DeLuca teaches the use of utilization limits as follows:

"...utilization limits..." at col. 12, lines 6-10.

"...utilization limits..." at col. 12, lines 6-10.

"...while remaining within said...utilization limits..." at col. 12, lines 6-10.

It would have been obvious to one ordinarily skilled in the art at the time of the invention to use hardware utilization limits in order to define the extent that hardware may be used without risking failure.

DeLuca does not teach the obtaining requirements from users, the use of workloads, the calculating of requirements, and the use of functions.

25. However, Shannon teaches obtaining requirements from users and calculating requirements as follows:

"...obtaining a...requirement from said human user..." at col. 1, lines 14-19.

"...calculating said...requirements..." at col. 2, lines 27-33.

"...requirement..." at col. 1, lines 14-19.

It would have been obvious to one ordinarily skilled in the art at the time of the invention to allow user input in order to provide the user with the capability of changing the previously defined data. Likewise, it would have been obvious to one ordinarily skilled in the art at the time of the invention to calculate the hardware resources required for a system in order to estimate the cost of hardware upgrades.

Shannon does not teach the use of workloads and the use of functions.

26. However, Litzenberger teaches the use of workloads as follows:

"...workload..." at col. 3, lines 27-29.

"...of said workload..." at col. 3, lines 27-29.

It would have been obvious to one ordinarily skilled in the art at the time of the invention to use workload requirements in order to determine how much work the computer hardware would be required to perform to justify hardware upgrades.

Litzenberger does not teach the use of functions.

27. However, Kulkarni teaches the use of functions as follows:

"...as a function..." at col. 1, lines 58-62.

It would have been obvious to one ordinarily skilled in the art at the time of the invention to use functions in order to establish relationships between component hardware parameters of a system and the performance of the system.

28. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coss, DeLuca, Shannon, Litzenberger, and Kulkarni as applied to claim 16 above, and further in view of Kayahara.

As per claim 17, the "...obtaining new...utilization limits...," is taught by DeLuca at col. 12, lines 6-10,

the "...hardware...," is taught by DeLuca at col. 5, lines 30-33,

the "...from said human user...," is taught by Shannon at col. 1, lines 14-19,

the "...recalculating said ...requirements...,' is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6,

the "...hardware...," is taught by DeLuca at col. 5, lines 30-33,

the "...while remaining within said...utilization limits...," is taught by DeLuca at col. 12, lines 6-10,

the "...hardware...," is taught by DeLuca at col. 5, lines 30-33,

the "...hardware requirements...," is taught by DeLuca at col. 6, lines 11-14,

the "...of the required hardware...," is taught by DeLuca at col. 6, lines 11-14,

the "...for the user entered...," is taught by Shannon at col. 1, lines 14-19,

the "...workload...," is taught by Litzenberger at col. 3, lines 27-29,

but the "...displaying...in a format to advice the user...," is not taught by either Coss, DeLuca, Shannon, Litzenberger, or Kulkarni.

However, Kayahara teaches the outputting of data in formats as follows:

"...Therefore, it is an object of the invention to dramatically decrease the burden of the searching operation which is performed by the user, make information searching possible by a searching method which the user desires, and make it possible to output a search result by categorizing and coordinating into a format the user desires..." at col. 1, lines 59-64.

It would have been obvious to one ordinarily skilled in the art at the time of the invention to output the results of the calculations in a defined format in order to provide the user feedback in a meaningful format.

29. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coss, DeLuca, Shannon, Litzenberger, Kulkarni, and Kayahara as applied to claim 17 above, and further in view of Leatham et al. (U.S. Patent No. 6,370,383).

As per claim 18, the "...hardware requirements...," is taught by DeLuca at col. 6, lines 11-14,

but the "...include discrete numbers of hardware components...," is not taught by either Coss, DeLuca, Shannon, Litzenberger, Kulkarni, or Kayahara.

However, Leatham teaches the use of discrete numbers of hardware components as follows:

"...Here, however, as each sectors 40-1 through 40-3 has a discrete number of radio transceivers serving that sectors, it is contemplated that, based on changes in the operation of the radio transceivers in each one of the sectors 40-1, 40-2 and 40-3, the MPT 46-1, 46-2 and 46-3 could be dramatically different for each respective sector 40-1, 40-2 and 40-3 of the sectored cell 40'..." at col. 15, lines 43-50.

"...Thus, the base station 14, the ICP 15 and the MSC 18 include a number of hardware and/or software components that are not described and illustrated herein..." at col. 7, lines 44-46.

It would have been obvious to one ordinarily skilled in the art at the time of the invention to use a discrete number of hardware components in order to have individually distinct hardware components and provide a more robust method of sizing a computer system.

30. As per claim 19, the "...calculating and recalculating steps include calculating...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6 and the "...said number of hardware components...," is taught by Leatham at col. 7, lines 44-46.

Conclusion

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harold E. Dodds, Jr. whose telephone number is (703)-305-1802. The examiner can normally be reached on Monday - Friday 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Breene can be reached on (703)-305-9790. The fax phone numbers for the organization where this application or proceeding is assigned are (703)-305-9730 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-305-3900.

Harold E. Dodds, Jr.
Patent Examiner
June 13, 2002

JOHN BREENE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100